DW_JUT

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Practice the sample paper covered both important questions and exam patterns

Subject: Analog and Digital Electronics (EEE304) **Full Marks: 70** **Time: 3 Hours**

Instructions:

- Question No. 1 is compulsory. (7 MCQs, 2 Marks each)
- Answer any FOUR questions from the remaining (Q.2 to Q.7).
- Q.2 to Q.6 carry 14 marks each (Divided into A and B, 7 Marks each).
- Q.7 consists of Short Notes (Answer any FOUR, 3.5 Marks each).

Q.1 Choose the correct option (Compulsory - 7 x 2 = 14 Marks)

i) How many flip-flops are required to design a Decade (Mod-10) counter?

a. 2

b. 3

c. 4

d. 10

ii) The majority charge carriers in an N-channel JFET are:

a. Holes

b. Electrons

c. Both electrons and holes

d. Ions

iii) Which parameter of an ideal Operational Amplifier should be infinite?

a. Output impedance

b. Common Mode Rejection Ratio (CMRR)

c. Offset voltage

d. None of the above

iv) The binary equivalent of the octal number $(23)_8$ is:

a. 10011
b. 010011
c. 101011
d. 011010

v) Which flip-flop is commonly known as a "transparent latch"?

a. S-R Flip-Flop
b. J-K Flip-Flop
c. T Flip-Flop
d. D Flip-Flop

vi) The ripple factor of a Half-Wave Rectifier is:

a. 0.48
b. 1.21
c. 1.11
d. 0.812

vii) The output of an XOR gate is HIGH (1) only when:

a. Both inputs are LOW
b. Both inputs are HIGH
c. Inputs are different (one HIGH, one LOW)
d. Inputs are identical

Answer any FOUR questions from Q.2 to Q.7

Q.2 A) Differentiate between BJT and JFET. Explain the construction and working principle of an N-channel JFET. *(7 Marks)*

Q.2 B) State and prove De Morgan's Theorems using logic symbols and truth tables. *(7 Marks)*

Q.3 A) Draw the block diagram of an OP-AMP. Explain its application as an Inverting and Non-Inverting Amplifier with necessary derivations for voltage gain. *(7 Marks)*

Q.3 B) Draw the logic diagram and explain the working of a 4-bit Asynchronous (Ripple) Binary Counter. Draw its timing diagram. *(7 Marks)*

Q.4 A) Explain the working principle of a Zener diode and draw its V-I characteristics. How does it act as a voltage regulator? *(7 Marks)*

Q.4 B) Simplify the following Boolean expression using a 3-variable Karnaugh Map (K-map) and implement it using basic logic gates: $F(A,B,C) = \Sigma m(0, 1, 2, 3, 4, 5)$. *(7 Marks)*

Q.5 A) Explain the working principle of a Successive Approximation Analog to Digital Converter (ADC) with a neat block diagram. *(7 Marks)*

Q.5 B) Discuss the internal block diagram of an IC 555 Timer. Explain its operation as an Astable Multivibrator. *(7 Marks)*

Q.6 A) Explain the working of a Full Adder circuit. Draw its logic diagram, truth table, and write the logic expressions for Sum and Carry. *(7 Marks)*

Q.6 B) (Numerical)

i) Subtract $(10)_{10}$ from $(25)_{10}$ using the 2's complement method.

ii) Convert $(75)_{10}$ to its Binary and Hexadecimal equivalents. *(7 Marks)*

Q.7 Write short notes on any FOUR of the following (4 x 3.5 = 14 Marks)

A. Shift Registers (SIPO & SISO)

B. D and T Flip-Flops

C. Opto-couplers and Photodiodes

D. Universal Gates

E. BCD to Seven Segment Decoder

SOLUTIONS FOR SAMPLE PAPER 3

MCQ Answer Key

i) c, **ii)** b, **iii)** b, **iv)** b, **v)** d, **vi)** b, **vii)** c

Model Answers for Long Questions

Q.2 A) BJT vs JFET & N-Channel JFET:

Differences: A Bipolar Junction Transistor (BJT) is a current-controlled device (I_C depends on I_B) and uses both electrons and holes. It has a low input impedance. A Junction Field Effect Transistor (JFET) is a voltage-controlled device (I_D depends on V_{GS}), uses only majority charge carriers (unipolar), and has extremely high input impedance.

N-Channel JFET Working: It consists of an N-type semiconductor channel with two P-type regions diffused on the sides (connected together as the Gate). The ends of the N-channel are the Drain and Source.

When a voltage V_{DS} is applied, electrons flow from Source to Drain. The Gate is always reverse-biased (negative voltage). As V_{GS} becomes more negative, the depletion regions around the P-N junctions widen into the N-channel. This narrows the conductive path, restricting the flow of electrons and reducing the Drain current (I_D). Thus, it acts as a voltage-controlled resistor.

Q.2 B) De Morgan's Theorems:

Theorem 1: The complement of a sum of variables is equal to the product of their complements.

Equation: $(A + B)' = A' \cdot B'$

This indicates that a NOR gate is logically equivalent to an AND gate with inverted inputs (Bubbled AND).

Theorem 2: The complement of a product of variables is equal to the sum of their complements.

Equation: $(A \cdot B)' = A' + B'$

This indicates that a NAND gate is logically equivalent to an OR gate with inverted inputs (Bubbled OR).

Q.3 A) OP-AMP Amplifiers:

Block Diagram: Input Stage (Dual-input, balanced-output differential amplifier) → Intermediate Stage → Level Shifter → Output Stage (Push-pull amplifier).
[Image of operational amplifier block diagram]
Inverting Amplifier: Input V_{in} is connected to the inverting terminal (-) via R_1, and non-inverting (+) is grounded. Feedback resistor R_f connects output to the inverting input. Due to virtual ground, the inverting terminal is at 0V.
$I_{in} = I_f \rightarrow (V_{in}/R_1) = -(V_{out}/R_f) \rightarrow$ Gain $A_v = -(R_f/R_1)$.
[Image of inverting operational amplifier circuit diagram]
Non-Inverting Amplifier: Input V_{in} is applied to the non-inverting terminal (+). Feedback is applied to the inverting terminal via a voltage divider (R_1 and R_f). By virtual short, voltage at inverting terminal is also V_{in}.
Voltage across R_1 is V_{in}. Therefore, current $I = V_{in}/R_1$. This same current flows through R_f.
$V_{out} = I(R_1 + R_f) = (V_{in}/R_1)(R_1 + R_f) \rightarrow$ Gain $A_v = 1 + (R_f/R_1)$.

[Image of non inverting operational amplifier circuit diagram]

Q.3 B) 4-bit Asynchronous Binary Counter:

Working: Also known as a ripple counter. It is constructed using four Toggle (T) flip-flops or JK flip-flops (with J=1, K=1). The external clock pulse is applied ONLY to the clock input of the first flip-flop (LSB, FF_0).
The output (Q_0) of the first flip-flop acts as the clock trigger for the second flip-flop (FF_1), and Q_1 clocks FF_2, and so on. Because the clock signal "ripples" sequentially through the flip-flops, they do not change state simultaneously (hence asynchronous).
The counter will count upwards from 0000 (decimal 0) to 1111 (decimal 15) and then reset back to 0000.

Q.4 A) Zener Diode & Voltage Regulation:

Principle: A Zener diode is a heavily doped PN junction designed to operate safely in the reverse breakdown region. When the reverse bias exceeds the Zener voltage (V_z), the strong electric field causes quantum tunneling (Zener breakdown), allowing large current to flow without destroying the diode.

Voltage Regulator: Connected in parallel with the load and a series resistor (R_s). Once in breakdown, the voltage across the Zener diode remains strictly constant at V_z. If the input voltage increases, the Zener conducts more current, dropping the excess voltage across R_s, keeping the load voltage constant.

Q.4 B) Karnaugh Map (K-map) Simplification:

Given: F(A,B,C) = Σm(0, 1, 2, 3, 4, 5)
Draw a 3-variable K-map. Place 1s in cells 0 (000), 1 (001), 2 (010), 3 (011), 4 (100), and 5 (101).
We can form two main groups:
1. A "Quad" (group of 4) consisting of cells 0, 1, 2, 3. In this quad, variables B and C change, but A remains 0 (A').
2. A "Quad" consisting of cells 0, 1, 4, 5. In this quad, variables A and C change, but B remains 0 (B').
Simplified Expression: **F = A' + B'**
Implementation: The expression A' + B' can be implemented using two NOT gates and one OR gate, or simply a single NAND gate (since (A · B)' = A' + B' by De Morgan's).

Q.5 A) Successive Approximation ADC:

Working: It is one of the fastest analog-to-digital converters. It consists of a Successive Approximation Register (SAR), a Digital-to-Analog Converter (DAC), and a voltage comparator.
The SAR starts by setting the Most Significant Bit (MSB) to 1 and all other bits to 0. The DAC converts this binary guess into an analog reference voltage. The comparator compares this DAC voltage with the actual unknown analog input voltage.
- If Input Voltage > DAC Voltage, the MSB is kept as 1.
- If Input Voltage < DAC Voltage, the MSB is reset to 0.
The SAR then moves to the next significant bit and repeats the process until the LSB is reached. The final binary word in the SAR is the digital equivalent of the analog input.

Q.5 B) IC 555 Timer - Astable Multivibrator:

Internal Block Diagram: Features three 5kΩ resistors (voltage divider providing 2/3 V_{cc} and 1/3 V_{cc}), an upper comparator, a lower comparator, an SR flip-flop, and an NPN discharge transistor.
Astable Operation: Astable means it has NO stable state; it continuously produces a square wave. An external capacitor C charges through resistors R_A and R_B. When the capacitor voltage hits 2/3 V_{cc}, the upper comparator sets the flip-flop, turning ON the discharge transistor. The capacitor then discharges through R_B until the voltage drops to 1/3 V_{cc}. At this point, the lower comparator resets the flip-flop, turning OFF the transistor, and the capacitor begins to charge again. The cycle repeats infinitely.

Q.6 A) Full Adder Circuit:

Working: A Full Adder computes the sum of three binary bits: A, B, and a Carry-In (C_{in}). It outputs a Sum (S) and a Carry-Out (C_{out}).

Expressions:

Sum (S) = $A \oplus B \oplus C_{in}$

$C_{out} = (A \cdot B) + (B \cdot C_{in}) + (A \cdot C_{in})$

Implementation: It is built using two Half Adders. The first Half Adder adds A and B. The second Half Adder adds the Sum of the first to C_{in} to produce the final Sum. The carries from both Half Adders are passed through an OR gate to generate the final C_{out}.

[Image of full adder logic diagram and truth table]

Q.6 B) Numerical Solutions:

i) Subtract $(10)_{10}$ from $(25)_{10}$ using 2's complement:

Operation: 25 - 10 = 25 + (-10).

Binary of 25 = 011001.

Binary of 10 = 001010.

1's complement of 10 = 110101.

2's complement of 10 = 110101 + 1 = 110110.

Add 25 and 2's comp of 10:

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  011001
+ 110110
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 1001111
```

Discard the extra carry (1). The result is 001111, which equals $(15)_{10}$. Correct!

ii) Convert $(75)_{10}$ to Binary and Hexadecimal:

To Binary: Successive division by 2.

75 / 2 = 37 (rem 1)

37 / 2 = 18 (rem 1)

18 / 2 = 9 (rem 0)

9 / 2 = 4 (rem 1)

4 / 2 = 2 (rem 0)

2 / 2 = 1 (rem 0)

1 / 2 = 0 (rem 1)

Binary = $\mathbf{(1001011)_2}$

To Hexadecimal: Group binary into 4-bit blocks from right to left.

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0100 | 1011
  4      B (11)
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Hexadecimal = $\mathbf{(4B)_{16}}$

Short Answer Solutions (Q.7)

A) Shift Registers (SIPO & SISO): Registers are groups of flip-flops used to store/transfer data. SISO (Serial-In Serial-Out) accepts data one bit at a time and outputs one bit at a time, creating a time delay. SIPO (Serial-In Parallel-Out) accepts data serially but makes it available on parallel output lines simultaneously, useful for serial-to-parallel conversion.

B) D and T Flip-Flops: The D (Data) flip-flop passes its input D to output Q on the clock pulse; it prevents the invalid state of the SR flip-flop. The T (Toggle) flip-flop changes its output state (toggles) every time the clock triggers if T=1; it is heavily used in binary counters.

C) Opto-couplers and Photodiodes: A photodiode generates current proportional to incident light when reverse-biased. An opto-coupler pairs an LED with a photodiode/phototransistor in a closed package. It allows electrical signals to be transmitted via light, providing perfect electrical isolation between sensitive low-voltage and noisy high-voltage circuits.

D) Universal Gates: NAND and NOR gates are termed universal because any combination of basic logic gates (AND, OR, NOT) and any complex Boolean function can be constructed using only NAND gates or only NOR gates, reducing manufacturing complexity.

E) BCD to Seven Segment Decoder: It is a combinational logic circuit that takes a 4-bit Binary Coded Decimal (BCD) number as input and activates the corresponding output lines (a through g) to display the decimal digit (0-9) on a 7-segment LED display. IC 7447 is a classic example.
