DW_JUT

DIPLOMA WALLAH

JHARKHAND UNIVERSITY OF TECHNOLOGY (JUT)

Practice the sample paper covered both important questions and exam patterns

Subject: Analog and Digital Electronics (EEE304) **Full Marks: 70** **Time: 3 Hours**

Instructions:

- Question No. 1 is compulsory. (7 MCQs, 2 Marks each)
- Answer any FOUR questions from the remaining (Q.2 to Q.7).
- Q.2 to Q.6 carry 14 marks each (Divided into A and B, 7 Marks each).
- Q.7 consists of Short Notes (Answer any FOUR, 3.5 Marks each).

Q.1 Choose the correct option (Compulsory - 7 x 2 = 14 Marks)

i) The maximum theoretical efficiency of a Full-Wave Rectifier is approximately:

a. 40.6%
b. 81.2%
c. 100%
d. 50%

ii) In a BJT, which configuration provides the highest power gain?

a. Common Base (CB)
b. Common Collector (CC)
c. Common Emitter (CE)
d. All provide equal gain

iii) Pin 6 of the IC 555 Timer is known as the:

a. Trigger pin
b. Discharge pin
c. Threshold pin
d. Reset pin

iv) Which of the following Analog to Digital Converters (ADC) is the fastest?

a. Successive Approximation ADC
b. Dual Slope ADC
c. Counter type ADC
d. Flash type ADC

v) According to Boolean Algebra, the expression A + AB simplifies to:

a. B
b. A
c. 1
d. 0

vi) The Common Mode Rejection Ratio (CMRR) of an ideal OP-AMP should be:

a. Zero
b. Unity
c. Infinite
d. Dependent on the supply voltage

vii) Which logic gate is also known as an "Inequality Gate"?

a. AND gate
b. OR gate
c. XOR gate
d. XNOR gate

Answer any FOUR questions from Q.2 to Q.7

Q.2 A) Explain the working of a Center-Tapped Full-Wave Rectifier with a neat circuit diagram and input/output waveforms. Mention its peak inverse voltage (PIV). *(7 Marks)*

Q.2 B) Simplify the following Boolean expression using a Karnaugh Map (K-map) and implement the simplified expression using basic logic gates: F(A,B,C) = Σm(1, 3, 5, 7). *(7 Marks)*

Q.3 A) Explain the working of a 4-bit Serial-In Parallel-Out (SIPO) Shift Register with a neat logic diagram. How many clock pulses are required to store a 4-bit word? *(7 Marks)*

Q.3 B) Draw the internal block diagram of an IC 555 Timer and explain its working as a Monostable Multivibrator. *(7 Marks)*

Q.4 A) Draw the logic diagram and explain the working of a Decade (Mod-10) Asynchronous Counter. Draw its truth table. *(7 Marks)*

Q.4 B) With the help of circuit diagrams, explain how an OP-AMP can be used as a Differentiator and a Summing Amplifier (Adder). *(7 Marks)*

Q.5 A) Explain the working principle of a Dual Slope Analog to Digital Converter (ADC) with a suitable block diagram. Mention its advantages. *(7 Marks)*

Q.5 B) Draw the input and output characteristics of a Bipolar Junction Transistor (BJT) in Common Emitter (CE) configuration. Clearly mark the cutoff, active, and saturation regions. *(7 Marks)*

Q.6 A) State and prove De Morgan's Theorems. Show how basic logic gates (AND, OR, NOT) can be implemented using only NAND gates. *(7 Marks)*

Q.6 B) (Numerical)
i) Subtract 9 from 14 using the 1's complement method.
ii) Convert the decimal number $(255)_{10}$ to its Hexadecimal, Binary, and Octal equivalents. *(7 Marks)*

Q.7 Write short notes on any FOUR of the following (4 x 3.5 = 14 Marks)

A. Opto-couplers and Photodiodes
B. Zener Diode breakdown mechanism
C. BCD to Seven Segment Decoder
D. CMRR and Slew Rate of an OP-AMP
E. D Flip-Flop and its truth table

SOLUTIONS FOR SAMPLE PAPER 2

MCQ Answer Key

i) b, **ii)** c, **iii)** c, **iv)** d, **v)** b, **vi)** c, **vii)** c

Model Answers for Long Questions

Q.2 A) Center-Tapped Full-Wave Rectifier:

Working: It uses a transformer with a center-tapped secondary winding and two diodes (D_1 and D_2).
During the positive half cycle of the input AC, the upper end of the secondary is positive, making diode D_1 forward-biased. D_1 conducts current through the load. Meanwhile, the lower end is negative, making D_2 reverse-biased.
During the negative half cycle, the lower end becomes positive, forward-biasing D_2, while D_1 becomes reverse-biased. D_2 now conducts current through the load in the SAME direction. Thus, full-wave rectification is achieved.

Peak Inverse Voltage (PIV): The maximum reverse voltage across the non-conducting diode is $2V_m$.

Q.2 B) Karnaugh Map (K-map) Simplification:

Given: F(A,B,C) = Σm(1, 3, 5, 7)
Draw a 3-variable K-map (A on vertical, BC on horizontal). Place 1s in cells 1 (001), 3 (011), 5 (101), and 7 (111).
All four 1s are located in the right half of the K-map where the variable C is 1. They form a single "Quad" (group of 4).
Checking the variables for this quad: A changes from 0 to 1, B changes from 0 to 1, but C remains constant at 1.
Simplified Expression: **F = C**
Implementation: The output F is simply connected directly to input C. No basic gates are required, just a straight wire!

Q.3 A) 4-bit Serial-In Parallel-Out (SIPO) Shift Register:

Working: A SIPO shift register is used to convert serial data into parallel data. It consists of four D flip-flops connected in cascade (the Q output of one is connected to the D input of the next). All flip-flops share a common clock signal.
Data is applied serially to the D input of the first flip-flop. With each clock pulse, the data bit shifts one position to the right.
To store a 4-bit word (e.g., 1011), exactly **4 clock pulses** are required. After the 4th clock pulse, all 4 bits are fully loaded into the flip-flops and are available simultaneously on the 4 parallel output lines (Q_0, Q_1, Q_2, Q_3).

Q.3 B) IC 555 Timer - Monostable Multivibrator:

Internal Block Diagram: Contains three 5kΩ resistors forming a voltage divider (2/3 V_{cc} and 1/3 V_{cc}), two comparators, an SR flip-flop, and a discharge transistor.
Monostable Operation: It has only ONE stable state (LOW). When a negative trigger pulse is applied to Pin 2 (falling below 1/3 V_{cc}), the lower comparator sets the flip-flop, making the output HIGH. The external capacitor C starts charging through resistor R. When the capacitor voltage reaches 2/3 V_{cc}, the upper comparator resets the flip-flop. The output goes LOW, and the transistor discharges the capacitor. The circuit waits in this stable state until the next trigger.
Pulse Width (T) = $1.1 \times R \times C$.

Q.4 A) Decade (Mod-10) Asynchronous Counter:

Working: A decade counter counts from 0000 (0) to 1001 (9) and then resets to 0000. It is built using four JK flip-flops (configured to toggle, J=1, K=1) acting as a 4-bit ripple counter, which normally counts to 15.
To truncate the count at 10 (1010 in binary), a NAND gate is used. The inputs to the NAND gate are connected to the Q outputs of FF_1 and FF_3 (which are HIGH at count 10). The output of the NAND gate is connected to the asynchronous CLEAR inputs of all flip-flops. As soon as the counter hits 1010, the NAND gate outputs a 0, instantly clearing the counter back to 0000.

Q.4 B) OP-AMP as Differentiator and Adder:

Differentiator: Input is applied through a capacitor C to the inverting terminal, with a feedback resistor R_f.
Current $I_{in} = C(dV_{in}/dt)$. Using virtual ground, $I_{in} = I_f$. So, $C(dV_{in}/dt) = -(V_{out}/R_f)$.
$V_{out} = -R_f C (dV_{in}/dt)$. Output is proportional to the derivative of the input.
[Image of OP-AMP differentiator circuit]
Summing Amplifier (Adder): Multiple inputs (V_1, V_2, V_3) are applied through resistors (R_1, R_2, R_3) to the inverting terminal.
By KCL at the inverting node: $I_f = I_1 + I_2 + I_3$.
$V_{out} = -R_f \times [(V_1/R_1) + (V_2/R_2) + (V_3/R_3)]$. If $R_1=R_2=R_3=R_f$, then $V_{out} = -(V_1 + V_2 + V_3)$.

Q.5 A) Dual Slope ADC:

Working: It uses an integrator, a comparator, and a counter. It operates in two phases: Run-up and Run-down. First, the unknown analog input voltage is integrated for a fixed time interval. Then, a known reference voltage of opposite polarity is applied, discharging the integrator back to zero. The time it takes to reach zero is directly proportional to the unknown input voltage. This discharge time is measured by the digital counter to produce the digital output.
Advantages: High resolution and excellent noise rejection (because it averages out the noise over the integration period).

Q.5 B) BJT Characteristics (CE Configuration):

Input Characteristics: Plot of Base Current (I_B) vs Base-Emitter Voltage (V_{BE}) at constant Collector-Emitter Voltage (V_{CE}). It looks like a forward-biased diode curve.
Output Characteristics: Plot of Collector Current (I_C) vs V_{CE} for different values of I_B.
- **Cutoff Region:** $I_B = 0$, both junctions reverse biased. Transistor is OFF.
- **Active Region:** Flat, horizontal curves where I_C is proportional to I_B. Used for amplification.
- **Saturation Region:** The steep vertical part near $V_{CE} = 0$. Both junctions are forward biased. Transistor is fully ON.

Q.6 A) De Morgan's Theorems & NAND as Universal Gate:

Theorem 1: (A + B)' = A' · B' (Complement of sum is product of complements).
Theorem 2: (A · B)' = A' + B' (Complement of product is sum of complements).
Basic Gates using NAND:
- **NOT Gate:** Tie both inputs of a NAND gate together. Output = (A · A)' = A'.
- **AND Gate:** Use two NAND gates. Output of first is (A · B)'. Pass this through a second NAND (acting as NOT) to get A · B.
- **OR Gate:** Invert inputs A and B using two NAND gates to get A' and B'. Feed these to a third NAND gate. Output = (A' · B')', which by De Morgan's is A + B.

Q.6 B) Numerical Solutions:

i) Subtract 9 from 14 using 1's complement:

Operation: 14 + (-9).

Binary of 14 = 1110. Binary of 9 = 1001.

1's complement of 9 = 0110.

Add 14 and 1's complement of 9:

```
  1110
+ 0110
---------
1 0100 → End-around carry! We take the extra 1 and add it back to the LSB.
  0100
+    1
---------
  0101 → which is (5)10. Correct!
```

ii) Convert $(255)_{10}$ to Hexadecimal, Binary, and Octal:

To Hexadecimal: 255 / 16 = 15 with remainder 15 (F). 15 / 16 = 0 with remainder 15 (F). Result = $\mathbf{(FF)_{16}}$

To Binary: Convert each F to 4-bit binary. F = 1111. Result = $\mathbf{(11111111)_2}$

To Octal: Group the binary into 3 bits from right to left.

```
011 | 111 | 111
 3     7     7
```

Result = $\mathbf{(377)_8}$

Short Answer Solutions (Q.7)

A) Opto-couplers and Photodiodes: A photodiode converts light into electric current when operated in reverse bias. An opto-coupler (or opto-isolator) combines a light-emitting diode (LED) and a photodiode/phototransistor in a single package. It transfers electrical signals via light waves, providing excellent electrical isolation between high-voltage and low-voltage circuits.

B) Zener Diode breakdown mechanism: Occurs in heavily doped PN junctions. Because the depletion layer is very narrow, a strong electric field is created across it even at low reverse voltages. This strong field pulls electrons directly out of their covalent bonds (quantum tunneling), creating a large reverse current. This is called Zener breakdown.

C) BCD to Seven Segment Decoder: A combinational logic circuit that accepts a 4-bit Binary Coded Decimal (BCD) input and generates 7 output signals to drive a 7-segment LED display. IC 7447 is a common example used for common anode displays.

D) CMRR and Slew Rate of an OP-AMP:
- CMRR (Common Mode Rejection Ratio): The ratio of differential gain (A_d) to common mode gain (A_c). Ideal is infinity. It indicates the OP-AMP's ability to reject noise common to both inputs.
- Slew Rate: The maximum rate of change of output voltage with respect to time (V/µs). It dictates how fast the output can follow the input. Ideal is infinity.

E) D Flip-Flop and its truth table: Also known as Data or Delay flip-flop. It has only one data input (D). The output Q simply follows the input D at the active clock edge. It removes the invalid state of the SR flip-flop.
Truth Table: If D=0, Q=0 (Reset). If D=1, Q=1 (Set).
