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Practice the sample paper covered both important questions and exam patterns

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Subject: Analog and Digital Electronics (EEE304)   **Full Marks: 70**   **Time: 3 Hours**

Instructions:

- Question No. 1 is compulsory. (7 MCQs, 2 Marks each)
- Answer any FOUR questions from the remaining (Q.2 to Q.7).
- Q.2 to Q.6 carry 14 marks each (Divided into A and B, 7 Marks each).
- Q.7 consists of Short Notes (Answer any FOUR, 3.5 Marks each).

Q.1 Choose the correct option (Compulsory - 7 x 2 = 14 Marks)

i) In a Bipolar Junction Transistor (BJT), the base region is:

    a. Heavily doped and wide

    b. Lightly doped and thin

    c. Moderately doped and wide

    d. Heavily doped and thin

ii) The radix or base of the hexadecimal number system is:

    a. 2

    b. 8

    c. 10

    d. 16

iii) The slew rate of an ideal operational amplifier is:

    a. Zero

    b. Unity

    c. Infinite

    d. Dependent on input voltage

iv) Which of the following digital logic families has the lowest power dissipation?

    a. TTL (Transistor-Transistor Logic)

    b. ECL (Emitter-Coupled Logic)

    c. CMOS (Complementary Metal-Oxide-Semiconductor)

    d. DTL (Diode-Transistor Logic)

v) A TRIAC can be considered as two SCRs connected in:

    a. Series

    b. Parallel

    c. Anti-parallel

    d. Cascade

vi) The Boolean expression $A + A'B$ is equivalent to:

    a. A

    b. B

    c. A + B

    d. AB

vii) In an intrinsic semiconductor at room temperature, the number of electrons and holes are:

    a. Zero

    b. Equal

    c. Unequal

    d. Infinite

Answer any FOUR questions from Q.2 to Q.7

Q.2 A) Explain the working of a Full-Wave Bridge Rectifier with a neat circuit diagram and waveforms. Calculate its efficiency and ripple factor. *(7 Marks)*

Q.2 B) Explain the working principle and construction of an N-channel enhancement MOSFET. Draw its transfer characteristics and compare it with a BJT. *(7 Marks)*

Q.3 A) Draw the block diagram of an OP-AMP. Explain its application as an Inverting Amplifier and an Integrator with necessary derivations. *(7 Marks)*

Q.3 B) What is a Multiplexer? Draw the logic diagram and truth table for a 4:1 Multiplexer (MUX). *(7 Marks)*

Q.4 A) Explain the operation of a Master-Slave J-K Flip-Flop. What is the race-around condition, and how does this flip-flop eliminate it? *(7 Marks)*

Q.4 B) What is a Karnaugh Map (K-map)? Simplify the Boolean expression $F(A,B,C) = \Sigma m(0, 2, 4, 6)$ using a K-map and implement it using basic gates. *(7 Marks)*

Q.5 A) Explain the working of a 4-bit Asynchronous Binary Counter with its block diagram, truth table, and timing diagram. *(7 Marks)*

Q.5 B) Discuss the pin diagram and internal block diagram of an IC 555 Timer. Explain its operation as an Astable Multivibrator. *(7 Marks)*

Q.6 A) Explain the working principle of a Successive Approximation Analog to Digital Converter (ADC) with a neat block diagram. *(7 Marks)*

Q.6 B) (Numerical)
i) Subtract 14 from 25 using the 2's complement method.
ii) Convert $(1A)_{16}$ to its Binary and Octal equivalents. *(7 Marks)*

Q.7 Write short notes on any FOUR of the following (4 x 3.5 = 14 Marks)

    A. CE (Common Emitter) Amplifier and its characteristics

    B. Universal Gates (NAND/NOR implementation)

    C. D and T Flip-Flops

    D. Ideal characteristics of an OP-AMP

    E. Binary Weighted Resistor DAC

SOLUTIONS FOR SAMPLE PAPER 1

MCQ Answer Key

i) b,   **ii)** d,   **iii)** c,   **iv)** c,   **v)** c,   **vi)** c,   **vii)** b

Model Answers for Long Questions

Q.2 A) Full-Wave Bridge Rectifier:

Working: It consists of four diodes arranged in a bridge. During the positive half cycle of the AC input, diodes D_1 and D_2 are forward biased and conduct, while D_3 and D_4 are reverse biased. Current flows through the load. During the negative half cycle, D_3 and D_4 are forward biased, and D_1 and D_2 are reverse biased. The current through the load flows in the same direction in both half cycles.

Efficiency: $\eta = (P_{dc} / P_{ac}) \times 100 \approx 81.2\%$

Ripple Factor: $\gamma = \sqrt{(I_{rms}/I_{dc})^2 - 1} \approx 0.48$

Q.2 B) N-channel Enhancement MOSFET:

Construction & Working: It consists of a p-type substrate with two heavily doped n+ regions (Source and Drain). A thin SiO_2 layer insulates the Gate electrode from the substrate. When $V_{GS} = 0$, no channel exists (normally off). When a positive V_{GS} is applied, it repels holes and attracts electrons towards the gate, creating an "induced" n-channel between Source and Drain, allowing current I_D to flow when V_{DS} is applied.

Comparison with BJT: MOSFET is a voltage-controlled device with extremely high input impedance (BJT is current-controlled with low input impedance). MOSFET is unipolar; BJT is bipolar.

Q.3 A) OP-AMP Block Diagram & Applications:

Block Diagram: Input Stage (Dual-input, balanced-output differential amplifier) → Intermediate Stage (Dual-input, unbalanced-output differential amp) → Level Shifting Stage → Output Stage (Push-pull amplifier).

[Image of OP-AMP block diagram]

Inverting Amplifier: Input is applied to the inverting terminal via R_1, non-inverting is grounded. Feedback resistor R_f is connected between output and inverting input. Using virtual ground concept, $I_{in} = I_f$, so $(V_{in}/R_1) = -(V_{out}/R_f)$. Gain $A_v = -(R_f/R_1)$.

Integrator: The feedback resistor is replaced by a capacitor C. $I_{in} = I_c$, so $(V_{in}/R) = -C(dV_{out}/dt)$. Integrating both sides: $V_{out} = -(1/RC) \int V_{in}\, dt$.

[Image of OP-AMP integrator circuit]

Q.3 B) 4:1 Multiplexer (MUX):

Concept: A multiplexer selects one of many input lines and routes it to a single output line based on the status of select lines.
A 4:1 MUX has 4 data inputs (D_0, D_1, D_2, D_3), 2 select lines (S_1, S_0), and 1 output (Y).

Truth Table & Logic:
- S_1=0, S_0=0 → Y = D_0
- S_1=0, S_0=1 → Y = D_1
- S_1=1, S_0=0 → Y = D_2
- S_1=1, S_0=1 → Y = D_3

Expression: $Y = S_1'S_0'D_0 + S_1'S_0D_1 + S_1S_0'D_2 + S_1S_0D_3$

[Image of 4:1 multiplexer logic diagram]

Q.4 A) Master-Slave J-K Flip-Flop & Race-Around Condition:

Race-Around Condition: In a standard JK flip-flop, if J=1 and K=1, the output toggles. If the clock pulse width is longer than the propagation delay of the flip-flop, the output will toggle multiple times within a single clock pulse, causing an unpredictable final state.

Elimination using Master-Slave: It consists of two SR flip-flops (Master and Slave) connected in series. The Master is positive-level triggered, and the Slave is negative-level triggered (inverted clock). When the clock is HIGH, the Master responds to J and K inputs, but the Slave is disabled. When the clock goes LOW, the Master is disabled, and the Slave transfers the Master's state to the final output. This prevents multiple toggling during a single clock pulse.

Q.4 B) Karnaugh Map (K-map) Simplification:

A K-map is a graphical method used to minimize Boolean expressions without using algebraic theorems.

Given: $F(A,B,C) = \Sigma m(0, 2, 4, 6)$

Placing 1s in the 3-variable K-map for cells 0 (000), 2 (010), 4 (100), and 6 (110).

These four 1s form a "Quad" (group of 4) spanning across the edges.

Looking at the variables: A changes, B changes, but C remains 0 (C').

Simplified Expression: $F = C'$

Implementation: This can be implemented simply using a single NOT gate taking input C to produce output F.

Q.5 A) 4-bit Asynchronous Binary Counter:

Working: Also known as a ripple counter. It uses four T flip-flops or JK flip-flops (with J=1, K=1 to toggle). The clock pulse is applied only to the LSB flip-flop (FF_0). The output (Q_0) of the first flip-flop acts as the clock input for the second (FF_1), and so on. Since the clock ripples through the flip-flops sequentially, it is called asynchronous.

It counts from 0000 (0) to 1111 (15) and then resets to 0000.

Q.5 B) IC 555 Timer - Astable Multivibrator:

Internal Block Diagram: It contains a voltage divider (three 5kΩ resistors), two comparators, an SR flip-flop, and a discharge transistor.

Astable Operation: It has no stable state and continuously switches between HIGH and LOW, generating a square wave. The external capacitor C charges through R_A and R_B until it reaches $(2/3)V_{cc}$. The upper comparator sets the flip-flop, discharging the capacitor through R_B and the internal transistor until it drops to $(1/3)V_{cc}$. The lower comparator then resets the flip-flop, and the cycle repeats automatically.

Q.6 A) Successive Approximation ADC:

Working: It consists of a comparator, a Successive Approximation Register (SAR), and a DAC. The SAR sets the MSB to 1 and the rest to 0. The DAC converts this binary value to an analog voltage (V_{DAC}) and compares it with the input analog voltage (V_{in}).

If $V_{in} > V_{DAC}$, the MSB remains 1. If $V_{in} < V_{DAC}$, the MSB is reset to 0. This process is repeated for the next significant bit until the LSB is reached. It is faster than ramp or counter-type ADCs.

Q.6 B) Numerical Solutions:

i) Subtract 14 from 25 using 2's complement:

Operation: 25 - 14 → 25 + (-14)

Binary of 25 = 011001

Binary of 14 = 001110

1's complement of 14 = 110001

2's complement of 14 = 110001 + 1 = 110010

Add 25 and 2's comp of 14:

  011001

+ 110010

 1001011

Discard the extra carry (1). The final result is 001011 which is $(11)_{10}$.

ii) Convert $(1A)_{16}$ to Binary and Octal:

To Binary: Replace each hex digit with a 4-bit binary.

1 = 0001, A (10) = 1010.

Binary = **$(00011010)_2$**

To Octal: Group the binary result into 3-bit groups from right to left.

000 | 011 | 010

0   3   2

Octal = **$(32)_8$**

Short Answer Solutions (Q.7)

A) CE Amplifier & Characteristics: The Common Emitter (CE) configuration has the emitter terminal common to both input and output. It provides both voltage gain and current gain, resulting in the highest power gain among BJT configurations. Input and output voltages are 180° out of phase. Input impedance is moderate, and output impedance is moderate to high.

B) Universal Gates: NAND and NOR are called universal gates because any logical function or basic gate (AND, OR, NOT) can be implemented using only NAND or only NOR gates. For example, a NOT gate is made by tying the two inputs of a NAND/NOR gate together.

C) D and T Flip-Flops:
- **D (Data) Flip-Flop:** Has a single input D. Output Q follows the input D at the clock edge. Used extensively in registers and memory.
- **T (Toggle) Flip-Flop:** Has a single input T. When T=1, the output toggles its state on the clock edge. When T=0, the output remains the same. Used in counters.

D) Ideal characteristics of an OP-AMP: An ideal OP-AMP has infinite open-loop voltage gain ($A_v = \infty$), infinite input impedance ($Z_{in} = \infty$) meaning it draws no current, zero output impedance ($Z_{out} = 0$), infinite bandwidth, and infinite Common Mode Rejection Ratio (CMRR = ∞).

E) Binary Weighted Resistor DAC: A type of Digital to Analog Converter that uses an OP-AMP summing amplifier. The input resistors are weighted in a binary progression (R, 2R, 4R, 8R). Each digital bit connects or disconnects its corresponding resistor to the OP-AMP. A disadvantage is that a wide range of highly precise resistor values is required for high-resolution DACs.

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