JHARKHAND UNIVERSITY OF TECHNOLOGY

DIPLOMA 3RD SEMESTER EXAMINATION

LOGIC DESIGN USING VERILOG (ECE 302)

Time: 3 Hours | **Full Marks: 70** | **SET: 3**

INSTRUCTIONS:

1. Question No. 1 is Compulsory.
2. Answer any **FOUR** questions from the remaining.
3. This set covers topics like ALU, FSM, and Encoders not covered in Set 1 & 2.

Q.1. MULTIPLE CHOICE QUESTIONS [2 × 7 = 14]

(i) Which system task is used to monitor signal changes in Verilog?

(a) $display
(b) $monitor
(c) $stop
(d) $finish

(ii) A Johnson Counter with 4 Flip-Flops has how many states?

(a) 4
(b) 8
(c) 16
(d) 2

(iii) Priority Encoder is a:

(a) Sequential Circuit
(b) Combinational Circuit
(c) Memory Device
(d) None

(iv) In a PAL (Programmable Array Logic):

(a) AND is fixed, OR is programmable
(b) AND is programmable, OR is fixed
(c) Both programmable
(d) Both fixed

(v) Which operator is used for concatenation in Verilog?

(a) &
(b) |
(c) {}
(d) []

(vi) A weighted resistor DAC uses resistors of values:

(a) R, R, R, R
(b) R, 2R, 3R, 4R
(c) R, 2R, 4R, 8R
(d) R, 2R, R, 2R

(vii) The resolution of an n-bit ADC is:

(a) 1/2^n
(b) 1/(2^n - 1)
(c) 2^n
(d) n

SECTION B (Long Answer Type)

Q.2. (a) Explain **Universal Shift Register** with a neat block diagram. How does it perform Shift Left, Shift Right, and Parallel Load operations? **[7]**

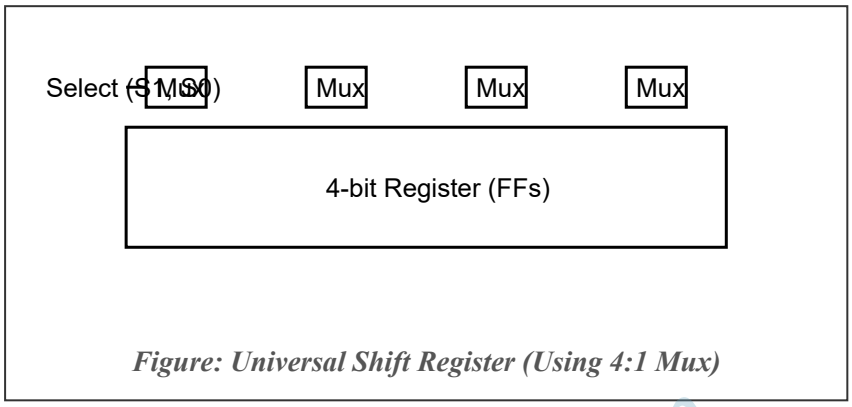

Figure: Universal Shift Register (Using 4:1 Mux)

Q.2. (b) Write the Verilog code for a **4-bit Arithmetic Logic Unit (ALU)** performing Addition, Subtraction, AND, OR using Case Statement. **[7]**

```
module ALU (input [3:0] A, B, input [1:0] Op, output reg [3:0] Y);
  always @(*) begin
    case(Op)
      2'b00: Y = A + B; // Add
      2'b01: Y = A - B; // Sub
      2'b10: Y = A & B; // AND
      2'b11: Y = A | B; // OR
    endcase
  end
endmodule
```


Q.3. (a) Explain **Johnson Counter (Twisted Ring Counter)** using D Flip-Flops. Draw logic diagram and timing waveforms for 4-bit. **[7]**

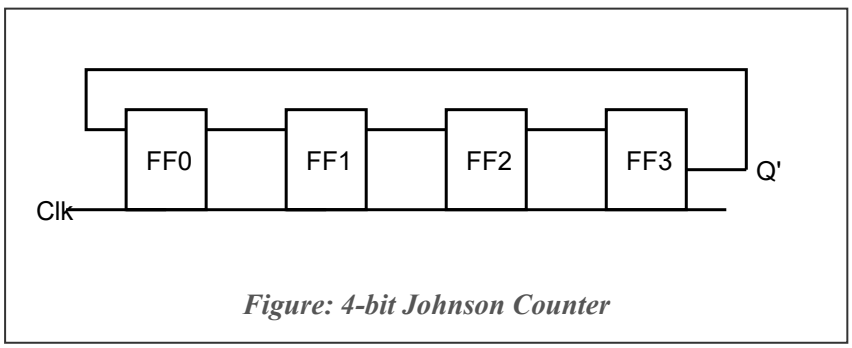

Figure: 4-bit Johnson Counter

Q.3. (b) Write Verilog code for **8:3 Priority Encoder** using `if-else` or `casex`. **[7]**

Q.4. (a) Explain **Weighted Resistor DAC**. What are its disadvantages compared to R-2R Ladder? **[7]**

Q.4. (b) Explain **Successive Approximation ADC**. Why is it widely used in microcontrollers? **[7]**

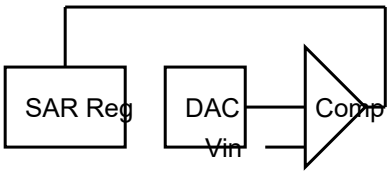

Figure: Successive Approximation ADC

Q.5. (a) Explain **D Flip Flop** and **T Flip Flop**. How can you convert a JK Flip Flop into a T Flip Flop? **[7]**

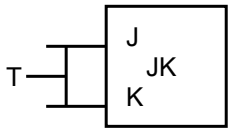

Figure: T Flip Flop from JK

Q.5. (b) Implement the following function using **PAL (Programmable Array Logic)**:
F1 = Σ(0, 1, 2)
F2 = Σ(2, 3) **[7]**

Q.6. [Long Answer] Design a **Sequence Detector** to detect the sequence **"101"** (overlapping allowed) using Mealy Machine.
(Steps: State Diagram, State Table, K-Map, Logic Diagram). **[14]**

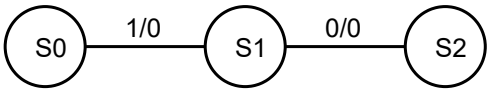

Figure: State Diagram Hint

Q.7. WRITE SHORT NOTES ON (ANY FOUR): [3.5 × 4 = 14]

a. Comparison of FPGA and CPLD
b. Dual Slope ADC (Integrating ADC)
c. Look Ahead Carry Adder (Concept)
d. Verilog System Tasks ($monitor, $display)
e. Difference between Latch and Flip Flop

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MCQ: (i) b, (ii) b, (iii) b, (iv) b, (v) c, (vi) c, (vii) b.

Q2(a) Hint: Universal Shift Register uses 4:1 Mux at input of each FF to select Hold, Shift Left, Shift Right, or Load.

Q3(a) Hint: Johnson counter inverts the last Qbar output and feeds it back to the first Flip Flop input.

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