JHARKHAND UNIVERSITY OF TECHNOLOGY

DIPLOMA 3RD SEMESTER EXAMINATION

LOGIC DESIGN USING VERILOG (ECE 302)

Time: 3 Hours **Full Marks: 70** **SET: 2**

INSTRUCTIONS:

1. Question No. 1 is Compulsory.
2. Answer any **FOUR** questions from the remaining.
3. Diagrams provided are for reference only. Draw them clearly in exam.

Q.1. MULTIPLE CHOICE QUESTIONS [2 × 7 = 14]

(i) Which logic gate is known as a Universal Gate?

(a) AND (b) OR
(c) NAND (d) XOR

(ii) In Verilog, which symbol represents Bitwise AND?

(a) && (b) &
(c) ~& (d) !

(iii) How many Flip-Flops are needed for a Mod-16 counter?

(a) 3 (b) 4
(c) 5 (d) 16

(iv) A Ring Counter with 4 Flip-Flops has how many states?

(a) 4 (b) 8
(c) 16 (d) 2

(v) PLA has:

(a) Fixed AND, Programmable OR (b) Programmable AND, Fixed OR
(c) Programmable AND, Programmable OR (d) Fixed AND, Fixed OR

(vi) The syntax `assign Y = A & B;` belongs to:

(a) Behavioral Modeling (b) Dataflow Modeling
(c) Structural Modeling (d) Gate Level

(vii) SIPO stands for:

(a) Serial In Parallel Out (b) Series In Parallel Out
(c) Serial Input Parallel Output (d) None

SECTION B (Long Answer Type)

Q.2. (a) Explain **SISO (Serial In Serial Out)** Shift Register using D Flip-Flops. Draw its logic diagram and timing diagram for data '1101'. [7]

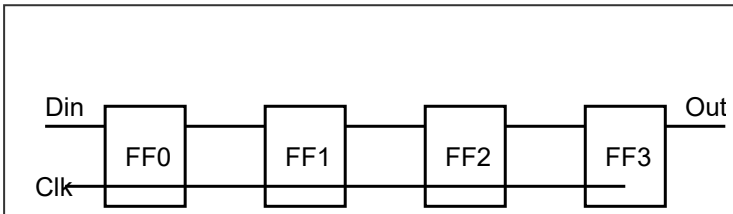

Figure: 4-bit SISO Shift Register

Q.2. (b) Write the Verilog code for a **1:4 Demultiplexer** using Dataflow Modeling. [7]

```
module demux1to4 (input I, input [1:0] S, output Y0, Y1, Y2, Y3);
  assign Y0 = I & ~S[1] & ~S[0];
  assign Y1 = I & ~S[1] & S[0];
  assign Y2 = I & S[1] & ~S[0];
  assign Y3 = I & S[1] & S[0];
endmodule
```

Q.3. (a) Explain **JK Flip Flop**. Convert **SR Flip Flop to JK Flip Flop** with necessary truth table and logic diagram. [7]

Q.3. (b) Write a Verilog code for **BCD to 7-Segment Decoder** using Behavioral Modeling (Case Statement). [7]

```
// Hint:
case (bcd)
  4'b0000 : seg = 7'b0000001; // 0
  4'b0001 : seg = 7'b1001111; // 1
  // ... continue for 0-9
endcase
```

Q.4. (a) Explain **Synchronous Counter**. Design a 3-bit Synchronous Up Counter using T Flip-Flops. [7]

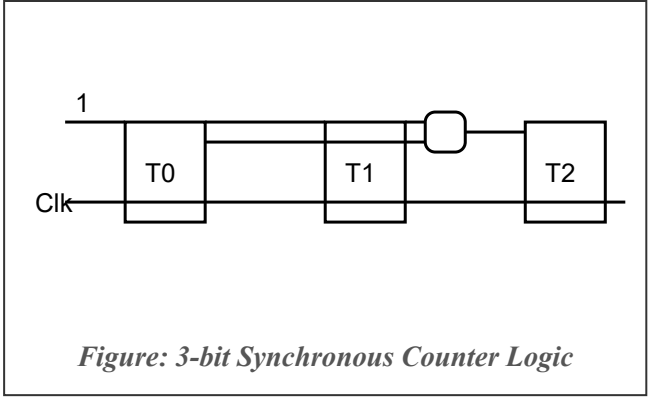

Figure: 3-bit Synchronous Counter Logic

Q.4. (b) Explain the difference between **Mealy Machine** and **Moore Machine** with state diagrams. **[7]**

Q.5. (a) Explain the architecture of **CPLD (Complex Programmable Logic Device)**. How is it different from FPGA? **[7]**

Q.5. (b) Explain **Flash Type ADC** (Parallel Comparator ADC). Why is it the fastest ADC? Draw its circuit for 2-bit conversion. **[7]**

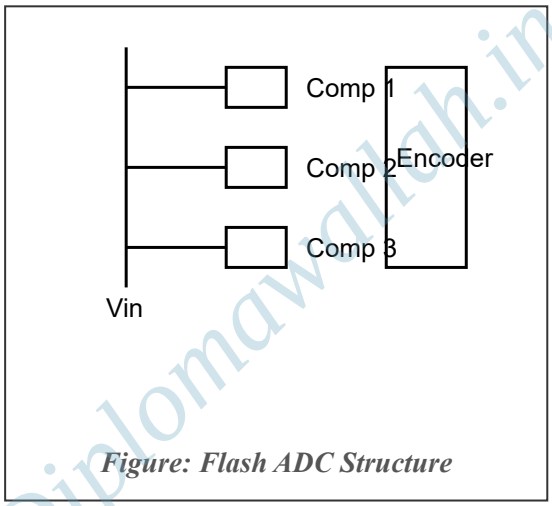

Figure: Flash ADC Structure

Q.6. Implement the following Boolean functions using **PLA (Programmable Logic Array)**: **[14]**

$$F1\ (A, B, C) = \Sigma\ m(0, 1, 2, 4)$$
$$F2\ (A, B, C) = \Sigma\ m(3, 5, 6, 7)$$

(Draw the PLA table and logic diagram showing connections in AND plane and OR plane).

Q.7. WRITE SHORT NOTES ON (ANY FOUR): [3.5 × 4 = 14]

a. Verilog Data Types (Wire vs Reg)
b. Blocking vs Non-Blocking Assignment
c. Ripple Counter vs Synchronous Counter
d. Successive Approximation ADC
e. User Defined Primitives (UDP)

DIPLOMA WALLAH: SOLUTION KEY

MCQ: (i) c, (ii) b, (iii) b, (iv) a, (v) c, (vi) b, (vii) a.

Q2(b) Hint: Use `assign` statement with logic equations for Dataflow modeling.

Q6 Hint: Minimize expressions using K-Map first, then implement on PLA grid.

Made With 💗 by Sangam (Diploma Wallah)