JHARKHAND UNIVERSITY OF TECHNOLOGY

Diploma 3rd Semester Examination

LOGIC DESIGN USING VERILOG (ECE 302)

Time: 3 Hours **Full Marks: 70** **SET: 1**

INSTRUCTIONS:

1. Question No. 1 is Compulsory.
2. Answer any **FOUR** questions from the remaining (Q.2 to Q.7).
3. Figures in the margin indicate full marks.

Q.1. Multiple Choice Questions [2 × 7 = 14]

(i) Which operator is used for "Non-Blocking Assignment" in Verilog?

(a) =
(b) <=
(c) ==
(d) assign

(ii) A JK Flip Flop toggles when:

(a) J=0, K=0
(b) J=1, K=0
(c) J=0, K=1
(d) J=1, K=1

(iii) FPGA stands for:

(a) Field Programmable Gate Array
(b) Fast Programmable Gate Array
(c) Field Processing Gate Array
(d) Flash Programmable Gate Array

(iv) Which modeling style uses "always" blocks?

(a) Data Flow
(b) Gate Level
(c) Behavioral
(d) Switch Level

(v) A Mod-10 counter requires minimum how many Flip-Flops?

(a) 3
(b) 4
(c) 5
(d) 10

(vi) Which is the fastest ADC?

(a) Successive Approximation
(b) Dual Slope
(c) Flash Type
(d) Counter Type

(vii) The output of a 2-input XOR gate is 1 when:

(a) Both inputs are same
(b) Both inputs are different
(c) Both inputs are high
(d) Both inputs are low

SECTION B (LONG ANSWER TYPE)

Q.2. (a) Explain the working of **Master-Slave JK Flip Flop** with a neat logic diagram. How does it eliminate the Race Around Condition? **[7]**

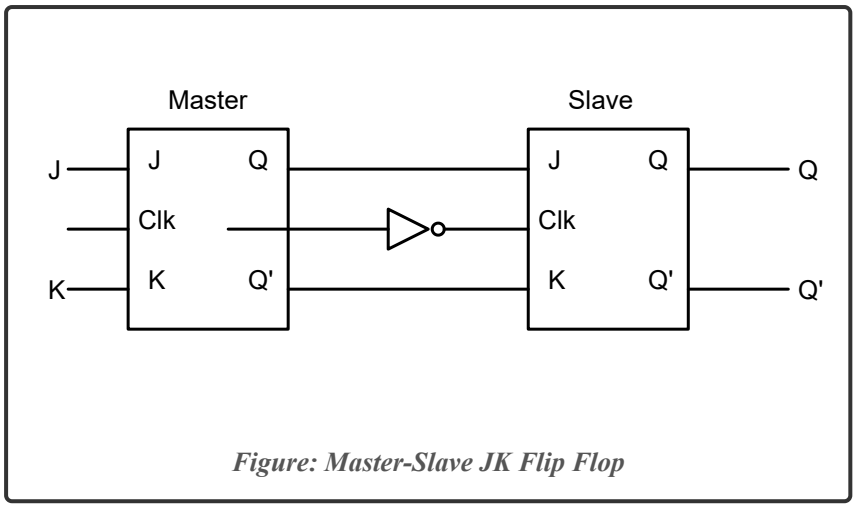

Figure: Master-Slave JK Flip Flop

Q.2. (b) Write the **Verilog code for a 4:1 Multiplexer** using Behavioral Modeling (Case Statement). **[7]**

```
// Hint Structure:
module mux4to1 (input [3:0] I, input [1:0] S, output reg Y);
  always @ (I, S)
  begin
    case (S)
      2'b00 : Y = I[0];
      // ... complete the cases
    endcase
  end
endmodule
```

Q.3. (a) Design a **Mod-10 Asynchronous (Ripple) Counter**. Draw its logic diagram and timing waveforms. **[7]**

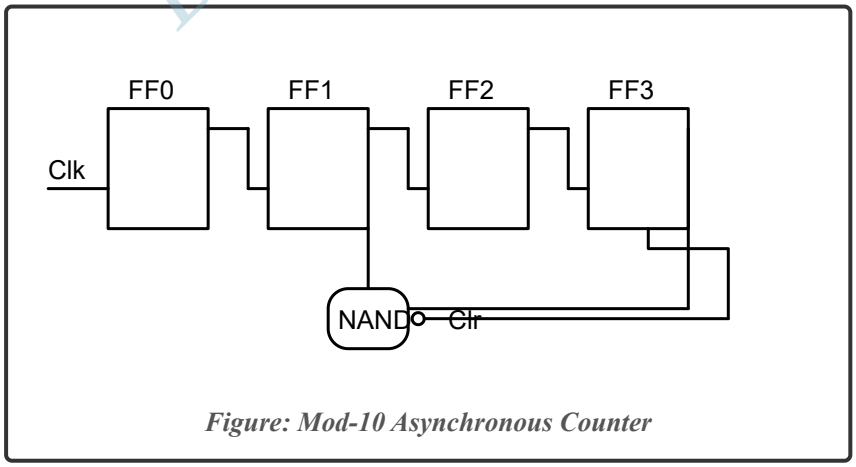

Figure: Mod-10 Asynchronous Counter

Q.3. (b) Differentiate between **Blocking (=)** and **Non-Blocking (<=)** assignments with suitable Verilog examples. **[7]**

Q.4. (a) Explain **4-bit Serial In Serial Out (SISO)** shift register using D Flip-Flops. Draw its logic diagram. **[7]**

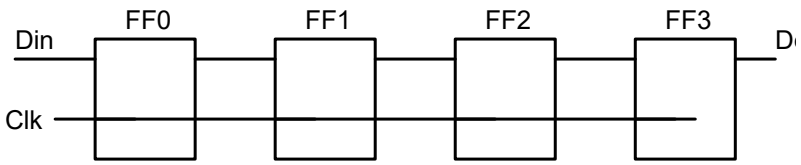

Figure: 4-bit SISO Shift Register

Q.4. (b) Write the Verilog code for a **Full Adder** using Gate Level Modeling. **[7]**

```
module Full_Adder(input A, B, Cin, output Sum, Carry);
  wire w1, w2, w3;
  xor G1(w1, A, B);
  xor G2(Sum, w1, Cin);
  and G3(w2, A, B);
  and G4(w3, w1, Cin);
  or G5(Carry, w2, w3);
endmodule
```

Q.5. (a) Explain the working of **R-2R Ladder DAC** with a neat circuit diagram. **[7]**

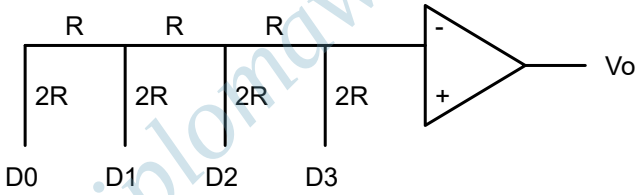

Figure: 4-bit R-2R Ladder DAC

Q.5. (b) Implement the following function using **PLA** (Programmable Logic Array):
F1(A, B, C) = Σ(0, 1, 2, 4) **[7]**

Q.6. Draw and explain the basic architecture of **FPGA** (Field Programmable Gate Array). Explain CLB and I/O blocks. **[14]**

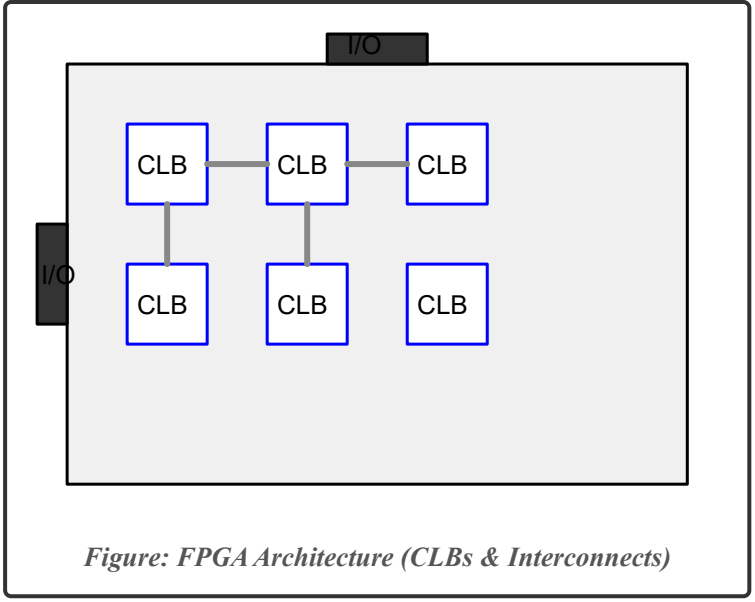

Figure: FPGA Architecture (CLBs & Interconnects)

Q.7. Write Short Notes on (Any FOUR): [3.5 × 4 = 14]

a. Race Around Condition in JK Flip Flop

b. Structural vs Behavioral Modeling

c. Universal Shift Register

d. Ring Counter

e. Verilog Data Types (Reg vs Wire)

✅ Diploma Wallah: Solutions Key

Q1 (MCQ Answers): (i) b, (ii) d, (iii) a, (iv) c, (v) b, (vi) c, (vii) b.

Q3(a) Hint: Mod-10 needs 4 FFs. Reset logic is connected to Q3(8) and Q1(2) because 8+2=10 (Binary 1010).

Q5(b) Hint: Convert minterms to binary. Mark connections in PLA grid (AND plane for minterms, OR plane for outputs).