

JHARKHAND UNIVERSITY OF TECHNOLOGY

DIPLOMA 3RD SEMESTER EXAMINATION

ANALOG ELECTRONICS (ECE 301)

DIPLOMA WALLAH

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Time: 3 Hours

Full Marks: 70

SET: 3

INSTRUCTIONS:

1. Question No. 1 is Compulsory.
2. Answer any **FOUR** questions from the remaining (Q.2 to Q.7).

Q.1. MULTIPLE CHOICE QUESTIONS

[2 × 7 = 14]

(i) A UJT is essentially a:

- (a) Current controlled device (b) Voltage controlled device
(c) Relaxation Oscillator (d) All of the above

(ii) The feedback fraction of Hartley Oscillator is decided by:

- (a) Capacitor divider (b) Inductor divider
(c) Resistor divider (d) Transistor beta

(iii) Op-Amp can be used as a summing amplifier in:

- (a) Inverting mode only (b) Non-inverting mode only
(c) Both modes (d) Saturation mode

(iv) Darlington Pair is used to achieve:

- (a) High Voltage Gain (b) High Current Gain
(c) High Bandwidth (d) Low Input Impedance

(v) Which class of amplifier conducts for less than 180 degrees?

- (a) Class A (b) Class B
(c) Class C (d) Class AB

(vi) A series voltage regulator uses a transistor in:

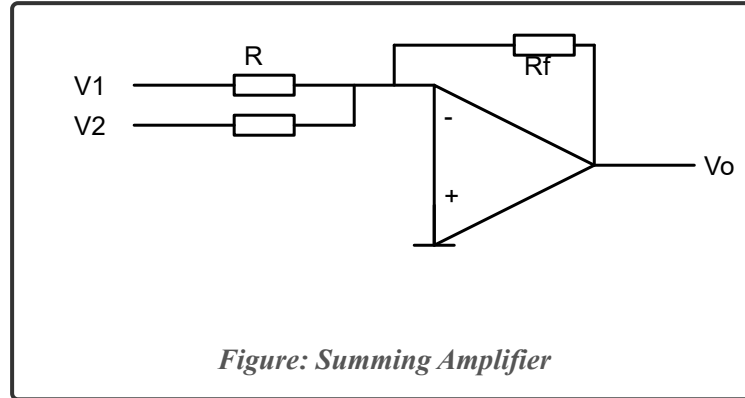
- (a) Series with Load (b) Parallel with Load
(c) Feedback loop (d) None

(vii) The maximum efficiency of a Centre-Tapped Full Wave Rectifier is:

- (a) 40.6% (b) 50%
(c) 81.2% (d) 100%

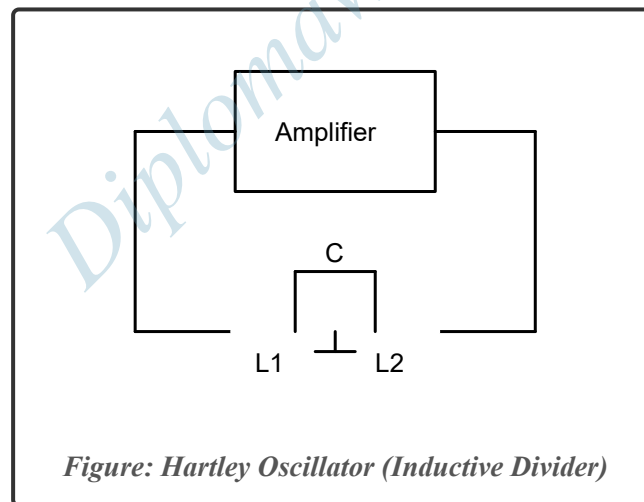
SECTION B (LONG ANSWER TYPE)

Q.2. (a) Explain the working of an **Op-Amp as a Summing Amplifier** (Adder) in inverting mode. Derive the expression: $V_o = -(V_1 + V_2 + V_3)$. [7]



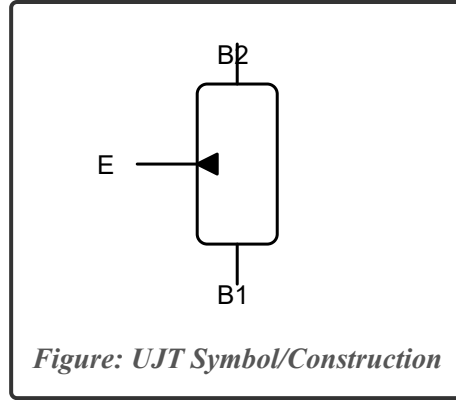
Q.2. (b) Draw and explain the working of a **Centre-Tapped Full Wave Rectifier**. Calculate its Ripple Factor and Efficiency. [7]

Q.3. (a) Draw the circuit diagram of **Hartley Oscillator**. Explain its operation and write the formula for frequency of oscillation. [7]



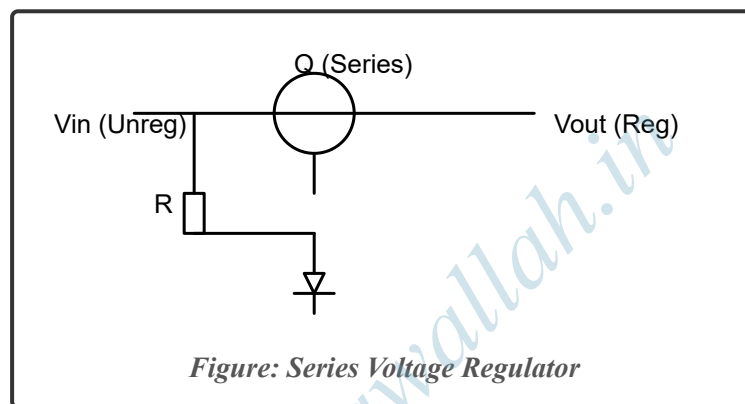
Q.3. (b) Explain **Colpitts Oscillator**. How does it differ from Hartley Oscillator? (Hint: Uses Capacitive Divider). [7]

Q.4. (a) Explain the construction and characteristics of **UJT (Uni-Junction Transistor)**. How is it used as a Relaxation Oscillator? [7]



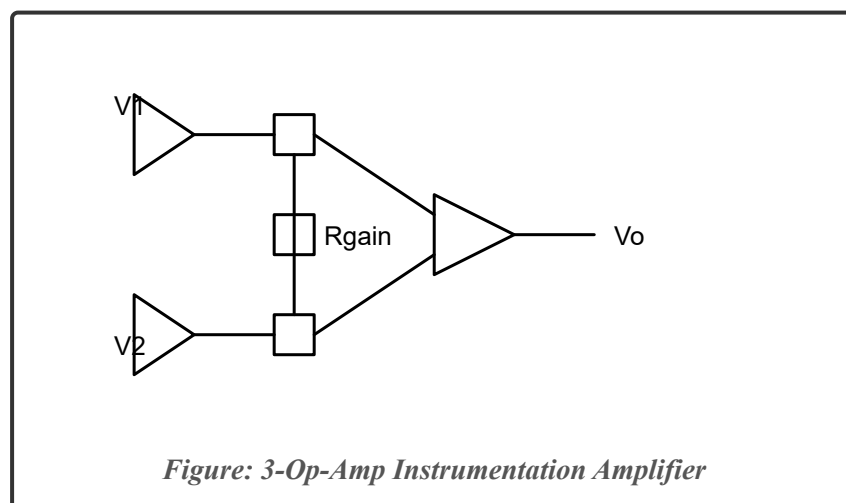
Q.4. (b) Explain **Load Line Analysis** (DC Load Line). What is the significance of the Q-point in amplification? [7]

Q.5. (a) Draw the circuit of a **Series Voltage Regulator** using a Transistor and Zener Diode. Explain its working. [7]



Q.5. (b) Explain **Voltage Doubler** circuit (Half Wave or Full Wave) with a neat diagram. [7]

Q.6. [Long Answer] Draw the circuit diagram of an **Instrumentation Amplifier** using 3 Op-Amps. Derive the expression for its output voltage. Why is it used in medical and industrial applications? [14]



Q.7. WRITE SHORT NOTES ON (ANY FOUR): [3.5 × 4 = 14]

a. Current Series Feedback

- b. Darlington Pair
 - c. LED vs LCD
 - d. Opto-Isolator
 - e. Band Pass Filter
-

✓ **SOLUTION KEY (PAPER 3)**

Q1 MCQ: (i) b (Double base), (ii) b, (iii) a, (iv) b, (v) c, (vi) a, (vii) c.

Q2(a) Hint: Current at inverting node is sum of currents: $I_1 + I_2 + I_3 = -I_f$. Leads to $V_o = -(V_1 + V_2 + V_3)$.

Q3(a) Hint: Hartley uses two Inductors (L_1, L_2) in series with parallel Capacitor.

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